

## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

### Listing of Claims:

1           1. (Original) A thin film transistor comprising:  
2           a buffer layer formed on a substrate;  
3           an activation layer formed on said buffer layer; and  
4           a gate insulation layer formed on said substrate including said activation layer,  
5           with said buffer layer having a step formed between a lower part of said activation layer and  
6           a part except said lower part of said activation layer, and said step being a half or less of the  
7           thickness sum of said activation layer and gate insulation layer.

1           2. (Original) The thin film transistor according to claim 1, wherein said buffer layer has a  
2           step to such a degree that thickness of said gate insulation layer is not changed on said side wall of  
3           said buffer layer.

1           3. (Currently Amended) The thin film transistor according to claim 1, wherein said activation  
2           layer comprising a solid-phase crystallization polysilicon, and a thickness of the gate insulation layer  
3           is at least 400 Å when a thickness of said solid-phase crystallization polysilicon is 300 Å and step  
4           is 350 Å in ~~the~~ said activation layer.

1           4. (Currently Amended) The thin film transistor according to claim 1, wherein said activation  
2 layer comprising an excimer laser annealing polysilicon, and thickness of the gate insulation layer  
3 is at least 1,000 Å when a thickness of said excimer laser annealing polysilicon is 500 Å and step  
4 is 750 Å in ~~the~~ said activation layer.

1           5. (Currently Amended) The thin film transistor according to claim 2, wherein said activation  
2 layer being a solid-phase crystallization polysilicon, and a thickness of the gate insulation layer is  
3 400 Å or more when a thickness of said solid-phase crystallization polysilicon is 300 Å and step is  
4 350 Å in ~~the~~ said activation layer.

1           6. (Currently Amended) The thin film transistor according to claim 2, wherein said activation  
2 layer being an excimer laser annealing polysilicon, and thickness of the gate insulation layer is 1,000  
3 Å or more when a thickness of said excimer laser annealing polysilicon is 500 Å and step is 750 Å  
4 in ~~the~~ said activation layer.

1           7. (Withdrawn) A method for fabricating said thin film transistor of claim 1, comprising the  
2 steps of:

3           depositing an amorphous silicon layer on a substrate equipped with buffer layer;  
4           forming a polycrystalline silicon layer by crystallizing said amorphous silicon layer;  
5           forming an activation layer by etching said polycrystalline silicon layer;

6           treating the surface of said activation layer; and  
7           depositing a gate insulation layer on said substrate,  
8           with etching time being controlled in said activation layer forming process and activation  
9   layer surface treatment process so that step between a lower part of gate in the buffer layer and a part  
10   except the lower part of said gate has a step value corresponding to a half or less of the thickness sum  
11   of said activation layer and gate insulation layer.

1           8. (Withdrawn) The method for fabricating a thin film transistor according to claim 7,  
2   wherein the etching time is controlled so that said buffer layer has a step to such a degree that  
3   thickness of said gate insulation layer is not changed on said side wall of said buffer layer.

1           9. (Withdrawn) The method for fabricating a thin film transistor according to claim 7,  
2   wherein the etching time is controlled to accommodate said buffer layer having a step corresponding  
3   to a half or less of the thickness sum of the activation layer and gate insulation layer.

1           10. (Withdrawn) The method for fabricating a thin film transistor according to claim 9,  
2   wherein the etching time is controlled so that said buffer layer has a step to such a degree that  
3   thickness of said gate insulation layer is not changed on said side wall of said buffer layer.

1           11. (Withdrawn) The method for fabricating a thin film transistor according to claim 7,  
2   wherein a thickness of said gate insulation layer is 400 Å or more when the thickness of solid-phase

3 crystallization polysilicon is 300 Å and step is 350 Å in said activation layer.

1 12. (Withdrawn) The method for fabricating a thin film transistor according to claim 7,  
2 wherein thickness of said gate insulation layer is 1,000 Å or more when the thickness of excimer  
3 laser annealing polysilicon is 500 Å and step is 750 Å in said activation layer.

1 13. (Original) A thin film transistor, comprising:  
2 a buffer layer;  
3 an activation layer formed on said buffer layer; and  
4 a gate insulation layer formed on said buffer layer and said activation layer,  
5 with said buffer layer having a step formed between a lower part of said activation layer and  
6 a part except said lower part of said activation layer, and said step being up to a half of the thickness  
7 sum of said activation layer and gate insulation layer.

1 14. (Original) The thin film transistor according to claim 13, with said step being controlled  
2 according to said gate insulation layer being deposited to an even thickness on a side wall of said  
3 activation layer.

1 15. (Currently Amended) The thin film transistor according to claim 13, with said activation  
2 layer comprising a solid-phase crystallization polysilicon, and a thickness of said gate insulation  
3 layer being at least 400 Å when a thickness of said solid-phase crystallization polysilicon is 300 Å

and step is 350 Å in said activation layer.

16. (Currently Amended) The thin film transistor according to claim 13, with said activation layer comprising an excimer laser annealing polysilicon, and a thickness of said gate insulation layer being at least 1,000 Å when a thickness of said excimer laser annealing polysilicon is 500 Å and step is 750 Å in said activation layer.

17. (Withdrawn) A method for fabricating a thin film transistor including a buffer layer, an activation layer formed on said buffer layer, and a gate insulation layer formed on said buffer layer and said activation layer, with said buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer, and said step being up to a half of the thickness sum of said activation layer and gate insulation layer, said thin film transistor comprising:

forming a polycrystalline silicon layer;  
forming an activation layer by etching said polycrystalline silicon layer;  
treating the surface of said activation layer; and  
depositing a gate insulation layer on said substrate,  
with etching time being controlled in the activation layer forming process and activation layer surface treatment process to accommodate a step between a lower part of a gate in said buffer layer and a part except the lower part of said gate having a step value corresponding up to a half of the thickness sum of said activation layer and gate insulation layer.

1           18. (Withdrawn) The method for fabricating a thin film transistor according to claim 17,  
2 wherein the etching time is controlled to accommodate said buffer layer including the step to such  
3 a degree where said gate insulation layer is deposited to an even thickness on a side wall of said  
4 activation layer.

1           19. (Withdrawn) The method for fabricating a thin film transistor according to claim 17,  
2 wherein the etching time is controlled to accommodate said buffer layer having a step corresponding  
3 up to half of the thickness sum of the activation layer and gate insulation layer.

1           20. (Withdrawn) The method for fabricating a thin film transistor according to claim 17,  
2 wherein a thickness of said gate insulation layer is at least 400 Å when the thickness of solid-phase  
3 crystallization polysilicon is 300 Å and the step is 350 Å in the activation layer or the thickness of  
4 said gate insulation layer is at least 1,000 Å when the thickness of excimer laser annealing  
5 polysilicon is 500 Å and the step is 750 Å in said activation layer.

1           21. (New) The thin film transistor according to claim 1, wherein a thickness of the gate  
2 insulation layer is at least 400 Å when a thickness of said activation layer is 300 Å and step is 350  
3 Å in said activation layer.

1           22. (New) The thin film transistor according to claim 1, wherein the step of said buffer layer

- 2 being formed on a single body of said buffer layer with the step protruding from a flat portion of  
3 said buffer layer and the step of said activation layer being formed on a single body of said activation  
4 layer with the step of said activation layer protruding from a flat portion of said activation layer.